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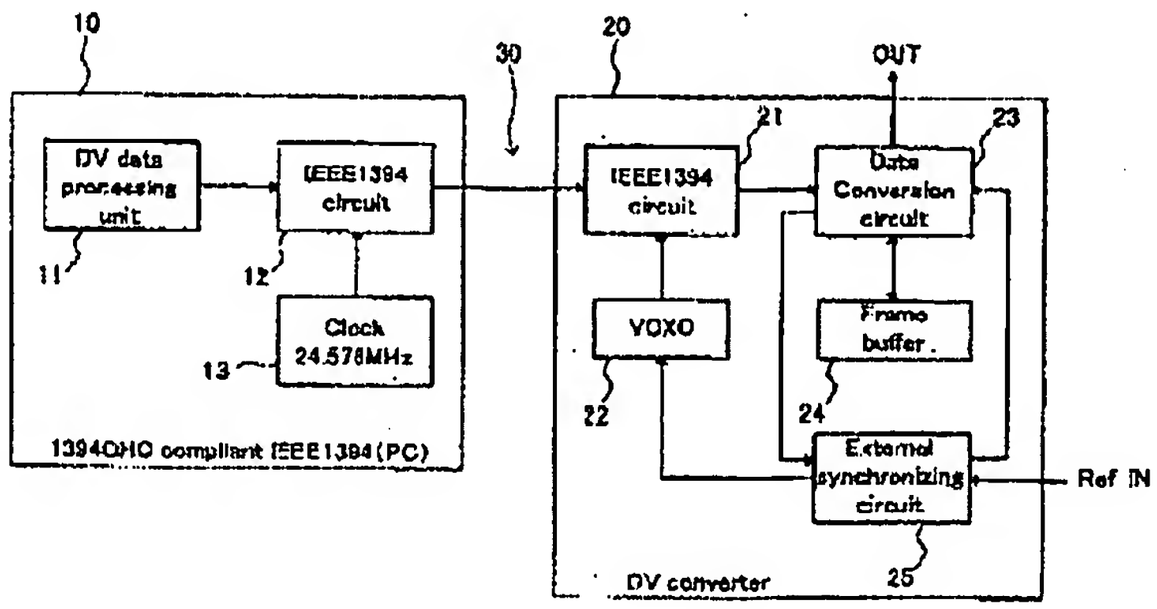
(54) DATA CONVERSION SYSTEM

(57) A data conversion system for converting data output from an information processor into data in a different format in real time while preventing image defects such as dropped frames or repeated frames in moving image data by synchronizing data transfer with converted data output. One of first and second nodes on an IEEE1394 bus functions as a cycle master, and first data is transferred from the first node to the second node in synchronism with a cycle start packet outputted from the cycle master. Second data generated by converting the first data by the second node is outputted in synchronism with an external reference signal. The system includes an external synchronizing signal receiver for receiving an external reference signal provided on at least one of the first and second nodes, and a synchronization adjustment unit for synchronizing the frequency of the cycle start packet output from the cycle master with the frequency of the reference signal received by the external synchronizing signal receiver

Fig. 1



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Description

Technical Field

[0001] The present invention relates to a data conversion system for real time conversion of data output from an information processor into data in a different format; more specifically, it relates to a data conversion system configured so that one of first and second nodes on an IEEE1394 bus serves as cycle master, first data is transferred from the first node to the second node in synchronism with a cycle start packet output from the cycle master, and second data generated by conversion of the first data by the second node is output in synchronism with an external reference signal.

Background Art

[0002] Due to remarkable improvements in the data recording capacity and processing speed of personal computers (PC), so-called nonlinear editing for performing video editing on a PC is becoming increasingly popular. For capturing video materials to a PC and outputting edited video images, dedicated hardware such as a video capture board, video editing board or the like is additionally inserted in an expansion slot, and data is input/output via such hardware.

[0003] Even today, handling analog video and high-end professional signals requires dedicated hardware. However, to handle just data in the DV (digital video) format, which is widely used for consumer devices and low-end professional use, even general inexpensive hardware meeting the standards for a 1394OHCI compliant IEEE 1394 interface is sufficient for practical use

[0004] This is because improvements in the CPU capacity of PCs have allowed the practical execution of such processing as video editing without having to use dedicated hardware, and an 1394OHCI compliant IEEE 1394 interface is now supported as an interface for a typical video editing software for input/output of data in DV format

[0005] A 1394OHCI compliant IEEE 1394 interface is frequently standard not only on desktop PCs but also on notebook PCs, enabling a single notebook PC to be used for everything from inputting/outputting to editing videos in DV format.

[0006] If only video material in DV format is to be handled, the process can be completed using a system as described above; however, there are many cases in which analog video images and material in SDI format for professional use need to be handled, and such cases require mutual conversion of formats. To perform mutual data conversion between video material in DV format and analog video images or video material in SDI format, an external unit type DV converter is often concurrently used, such converter converting an input analog video signal or SDI video signal to a DV format in real time and outputting the same as a DV signal, or conversely, converting a video signal in DV format to an analog video signal or SDI video signal and outputting the same.

[0007] There are various DV converters, ranging from those for consumer use to those for professional use. Professional use DV converters may require a function called external synchronization (genlock). With DV converters having no such external synchronization function, when a DV signal output from a PC via a 1394OHCI compliant IEEE1394 interface is converted into an analog video signal or SDI video signal, the converted analog video signal or SDI video signal is output at a timing in accordance with the frame frequency of the DV signal output from the PC

[0008] With DV converters having an external synchronization function, a reference signal that serves as a reference for output timing is input via a reference input terminal When a DV video signal output from a PC 1394OHCI compliant IEEE1394 interface is converted into an analog video signal or SDI video signal, the converted signal, while being buffered, is synchronized with the reference signal and output.

[0009] Data transmission between nodes connected on an IEEE1394 bus is either in an asynchronous transfer mode or isochronous transfer mode, and for video and audio transmission, isochronous transfer mode is used. This isochronous transfer mode is also used when a DV video signal is output via a PC 1394OHCI compliant IEEE1394 interface.

[0010] When a PC and DV converter exist on an IEEE1394 bus as nodes, and a DV video signal is to be output to the DV converter via a PC 1394OHCI compliant IEEE1394 interface, one of the PC and DV converter serves as a node called a cycle master for managing the transfer cycle, and cycle start packets are output to the IEEE1394 bus at a constant frequency (125μsec).

[0011] The PC 1394OHCI compliant IEEE1394 interface transmits a video signal in DV format in an IEEE1394 defined isochronous transfer packet format each time a cycle start packet output from the cycle master is detected

[0012] Thus, the frame frequency of the DV video signal output from a PC 1394OHCI compliant IEEE1394 interface is synchronized with the frequency of the cycle start packet output from the cycle master The interval of 125μsec between cycle start packets output from the cycle master is generated by frequency division at a set ratio from a 24.576MHz clock source of the node serving as cycle master. Because of differences in clock source for different pieces of hardware, frequency varies Therefore, because the frame frequency of a DV video signal output from a PC 1394OHCI compliant IEEE1394 interface differs depending on the device, a frame frequency on average will not match the frame frequency of an external reference signal input into a DV converter As a result, even when buffering is performed at the DV converter, there are problems such as dropped frames in output analog signals or SDI signals in cases where the PC transfer speed is high, and repeated frames in output

analog video signals or SDI video signals when the PC transfer speed is low.

[0013] The timing of the dropped frames or repeated frames is difficult to predict, and notwithstanding precise editing in frame units using video editing software loaded on a PC, there is the danger that defects such as dropped frames or repeated frames may irregularly occur in the images ultimately output

[0014] The present invention provides a data conversion system configured so that when data output from an information processor is converted into data in a different format in real time, data transfer and converted data output are synchronized, thereby preventing the occurrence of defects in moving image data such as dropped frames or repeated frames.

Disclosure of the Invention

[0015] The data conversion system according to claim 1 of the present invention is a data conversion system configured so that one of first and second nodes on an IEEE 1394 bus serves as cycle master, first data is transferred from the first node to the second node in synchronism with a cycle start packet output from the cycle master, and second data generated by conversion of the first data by the second node is synchronized with an external reference signal and output, and comprises an external synchronizing signal receiver for receiving an external reference signal provided on at least one of the first and second nodes; and a synchronization adjustment unit for synchronizing the cycle start packet frequency output from the cycle master with the frequency of the reference signals received by the external synchronizing signal receiver.

[0016] With this configuration, by synchronization of the cycle start packet frequency with the reference signal, the transfer rate of the data output from the first node can be matched to the output rate of the second data from the second node, thereby preventing the occurrence of dropped frames or repeated frames or the like in the output second data. In particular, when a video signal in DV format is converted into a video signal in a different format, the occurrence of any image defect such as dropped frames or repeated frame or the like can be prevented.

[0017] The data conversion system according to claim 2 of the present invention is the data conversion system according to claim 1, wherein the first node is hardware comprising a 1394OHCI compliant IEEE1394 interface for outputting a video signal in DV format as first data, and the second node is data conversion hardware for outputting an analog video signal or SDI video signal as second data

[0018] With this configuration, the output of video signals in DV format is output at a frequency in synchronism with the reference signal, thereby preventing the occurrence of image defects such as dropped frames or repeated frames in an analog video signal or SDI video signal

[0019] The data conversion system according to claim 3 of the present invention is the data conversion system according to either one of claim 1 or claim 2, wherein the second node has an external synchronizing signal receiver and synchronizing adjustment unit, and serves as cycle master for data transfer

[0020] With this configuration, the transfer rate of data output from the first node can be synchronized with a reference signal received by the second node

[0021] The data conversion system according to claim 4 of the present invention is a data conversion system according to either one of claim 1 or claim 2, wherein the first node has a synchronization adjustment unit, the second node has an external synchronizing signal receiver and synchronization adjustment unit, and the synchronization adjustment unit of the node serving as cycle master synchronizes the cycle start packet frequency with a reference signal received by the external synchronizing signal receiver.

[0022] With this configuration, whichever one of the first and second nodes serves as cycle master, data can be transferred in synchronism with the reference signal received by the external synchronizing signal receiver, thereby preventing occurrence of defects in data output from the second node.

[0023] The data conversion system according to claim 5 of the present invention is the data conversion system according to claim 4, wherein when the first node serves as cycle master, the synchronizing adjustment signal generated in accordance with the reference signal received by the external synchronizing signal receiver of the second node is transmitted from the second node to the first node by asynchronous transfer of the IEEE 1394 interface

[0024] With this configuration, because a synchronizing adjustment signal generated in accordance with the reference signal received by the external synchronizing signal receiver is transmitted using the IEEE1394 bus, even when the first node serves as cycle master, a synchronizing adjustment signal can be transmitted without increasing wiring

[0025] The data conversion system according to claim 6 of the present invention is a data conversion system according to claim 4, comprising a dedicated synchronization signal line for transmitting, from the second node to the first node, the synchronizing adjustment signal generated in accordance with the reference signal received by the external synchronizing signal receiver of the second node, the transmission performed in situations in which the first node serves as cycle master.

[0026] With this configuration, even when the external synchronizing reference signal is input in the second node and the first node serves as cycle master, the data transfer rate of the first node can be reliably synchronized with the reference signal.

[0027] The data conversion system according to claim 7 of the present invention is the data conversion system according to either one of claim 1 or claim 2, wherein the

first node has an external synchronizing signal receiver and synchronization adjustment unit, and serves as cycle master for data transfer.

[0028] With this configuration, because the frame frequency of data output from the first node is already fully externally synchronized, the second node only needs to perform conversion, enabling external synchronization so that the system overall does not have drop frame or repeated frame, even when the second mode is a DV converter with no external synchronization function

Brief Description of the Drawings

[0029]

FIG. 1 is a simplified block diagram of the first embodiment;
FIG. 2 is a simplified block diagram of the second embodiment; and
FIG. 3 is a simplified block diagram of the third embodiment.

Best Mode to Carry Out the Invention

[0030] In the present invention, a situation will be considered in which hardware (a PC) comprising a 1394OHCI compliant IEEE1394 interface, and conversion hardware ("DV converter") for converting a DV video signal output from the PC into an analog signal or SDI video signal and outputting the same, are connected as nodes on an IEEE 1394 bus The video signal in DV format output from the PC 1394OHCI compliant IEEE 1394 interface is transferred in an isochronous transfer mode to the DV converter that serves as a second node.

[0031] The isochronous transfer mode is managed by a node called a cycle master on the IEEE1394 bus, and in accordance with the cycle start packet that the cycle master outputs every 125μsec, a video signal in DV format is output from the PC 1394OHCI compliant IEEE1394 interface.

[0032] Because the interval between cycle start packets is determined by frequency division at a set ratio from a 24.576MHz clock source of the cycle master, and does not match the interval between reference signals input in an external synchronizing circuit, when an analog video signal or SDI video signal converted by the DV converter is output, defects arise such as dropped frames or repeated frames even if buffering is performed. Therefore, in the present invention, feedback control of the clock source frequency of the cycle master is carried out using the reference signal, causing the interval between cycle start packets output from the cycle master to be longer or shorter than 125μsec, and thereby dynamically changing the transfer rate of the IEEE1394, so that the average frame frequency of the video signal in DV format output from the 1394OHCI compliant IEEE 1394 interface matches the frequency of the external synchronizing reference signal

[0033] Hereinafter, the present invention will be explained with specific embodiments.

First Embodiment

[0034] The first embodiment of the present invention will be explained with reference to FIG. 1

[0035] In FIG 1, a PC 10 as 1394OHCI compliant IEEE1394 hardware, and a DV converter 20 for converting a video signal in DV format into an analog video signal or SDI video signal, are connected by an IEEE1394 cable 30.

[0036] The PC 10 comprises a DV data processing unit 11 containing a hard disk or other recording medium for storing moving image data in DV format, an IEEE1394 circuit 12 for inputting/outputting data in an IEEE1394-defined packet format, and a clock source 13 constituted by a crystal oscillator or the like The PC 10 contains a CPU, ROM, RAM, and other interfaces, but these functional parts are omitted in the drawing. The environment of the PC 10 allows for execution of a video editing software for editing at least data in DV format, and output can be made via the DV data processing unit 11 and IEEE1394 circuit 12.

[0037] The DV converter 20 comprises an IEEE1394 circuit 21 for receiving a video signal in DV format transferred via the IEEE1394 cable 30, a data conversion circuit 23 for converting the transferred video signal in DV format into an analog video signal or SDI video signal, a frame buffer 24 for temporally buffering the converted video signal, an external synchronizing circuit 25 for receiving an external reference signal, and a clock oscillator circuit VCXO (Voltage Controlled Crystal Oscillator) 22 subject to voltage feedback control by the external synchronizing circuit 25. This DV converter 20 also contains a CPU, ROM, RAM, and various interfaces, which are omitted in the drawing.

[0038] In the first embodiment thus configured, the IEEE1394 node constituted by the DV converter 20 serves as a cycle master The IEEE1394 circuit 21 of the DV converter 20 serving as the cycle master outputs a cycle start packet each 125μsec to the IEEE1394 bus, and the clock oscillator circuit for determining intervals between cycle start packets is controlled by the external synchronizing circuit 25.

[0039] The external synchronizing circuit 25 performs feedback control of VCXO 22 voltage to control VCXO 22 oscillation frequency so as to maintain a constant timing differential between the input reference signal and output analog video signal or SDI video signal With this configuration, the cycle start packet output interval generated by frequency division at a set rate of the VCXO 22 clock changes, and the transfer rate from the 1394OHCI compliant IEEE 1394 PC 10 determined by the cycle start packet interval is synchronized with the reference signal

[0040] With this configuration, the DV converter 20 receives transfer of a DV video signal from the PC 10

1394OHCI compliant IEEE1394 interface and completely synchronizes the data-converted analog video signal or SDI video signal with the reference signal and outputs the same in a state with no defects such as dropped frames or repeated frames

[0041] With the first embodiment, a standard product can be used as the IEEE1394 hardware PC 10

Second Embodiment

[0042] There are cases where it is not specified whether or not the IEEE1394 circuit in a PC connected to an IEEE1394 bus or the IEEE1394 circuit in a DV converter connected to the IEEE1394 is to serve as a cycle master When the DV converter does not serve as a cycle master, the PC IEEE1394 node serves as cycle master, and thus the PC clock oscillation frequency needs to be controlled so as to be synchronized with the reference signal. An explanation will be given with reference to FIG. 2 of such a case as a second embodiment of the present invention.

[0043] In FIG. 2, the PC 10 serving as 1394OHCI compliant IEEE1394 hardware and the DV converter 20 for converting a video signal in DV format into an analog video signal or SDI video signal are connected by the IEEE1394 cable 30.

[0044] The PC 10 comprises the DV data processing unit 11 containing a hard disk or other recording medium for storing moving image data in DV format, the IEEE1394 circuit 12 for inputting/outputting data in an IEEE-defined format, and the VCXO 14 subject to oscillation frequency control by voltage feedback. As with the above, the PC 10 contains a CPU, ROM, RAM, and other interfaces, but these functional parts are omitted in the drawing. Further, the PC 10 environment allows execution of a video editing software for editing at least data in DV format, and output is made via the DV data processing unit 11 and IEEE1394 circuit 12.

[0045] The DV converter 20 comprises the IEEE1394 circuit 21 for receiving a video signal in DV format transferred via the IEEE1394 cable 30, the data conversion circuit 23 for converting the transferred video signal in DV format into a video signal in an analog format or a video signal in an SDI format, the frame buffer 24 for temporally buffering the converted video signal, the external synchronizing circuit 25 for receiving the external reference signal, and the clock oscillator circuit VCXO 22 subject to voltage feedback control by the external synchronizing circuit 25. This DV converter 20 also comprises a CPU, ROM, RAM, and various interfaces, but these functional parts are omitted in the drawing.

[0046] With the second embodiment thus configured, when the IEEE1394 node that is the DV converter 20 serves as cycle master, as in the first embodiment, the external synchronizing circuit 25 performs feedback control of VCXO 22 voltage to control VCXO 22 oscillation frequency so as to maintain a constant timing differential between the input reference signal and output analog video signal or SDI video signal. With this configuration, the cycle start packet output interval generated by frequency division of the VCXO 22 clock at a set rate changes, and the transfer rate from the 1394OHCI compliant IEEE 1394 PC 10 determined by the cycle start packet interval is synchronized with the reference signal.

[0047] Further, when the IEEE1394 node that is the PC 10 serves as cycle master, the reference signal received by the external synchronizing circuit 25 of the DV converter is transmitted to the PC 10 via the IEEE1394 cable 30, and feedback control of the VCXO 14 in the PC 10 is performed so as to maintain a constant timing differential between the reference signal and cycle start packet. The reference signal can be transferred from the DV converter 20 to the PC 10 in an asynchronous transfer mode, and in such a case, the PC 10 requires an algorithm or the like for interpreting commands transmitted to the PC 10 by an AV/C protocol. With this configuration, the output interval between cycle start packets created by frequency division at a set rate of the VCXO 14 clock changes, and the transfer rate from the 1394OHCI compliant IEEE1394 PC 10 determined by the cycle start packet interval is also synchronized with the reference signal.

[0048] Thus, with the second embodiment, whether the PC 10 or DV converter 20 serves as cycle master, a data-converted analog video signal or SDI video signal is fully synchronized with the reference signal and output, in a state with no defects such as drop frame or repeated frame. Modification

[0049] In an alternative configuration, there is provided a separate dedicated control signal line 31 for transmitting to the PC 10 a synchronizing adjustment signal created in accordance with the reference signal input in the external synchronizing circuit 25 of the DV converter 20. In this case, the synchronizing adjustment signal created in accordance with the reference signal is reliably transmitted by the dedicated control signal line 31, and the VCXO14 in the PC 10 is subject to feedback control

Third Embodiment

[0050] In an alternative configuration, a reference signal for external synchronization is input in a PC, and the transfer frequency from the PC to the DV converter is controlled so as to be synchronized with this reference signal. An explanation will be given with reference to FIG 3 of such a case as a third embodiment.

[0051] In FIG. 3, the PC 10 serving as 1394OHCI compliant IEEE 1394 hardware and the DV converter 20 for converting a video signal in DV format into an analog video signal or SDI video signal are connected by the IEEE1394 cable 30

[0052] The PC 10 comprises the DV data processing unit 11 containing a hard disk or other recording medium for storing moving image data in DV format, the IEEE1394 circuit 12 for inputting/outputting data in an IEEE1394-defined packet format, the VCXO 14 subject to oscillation frequency control by voltage feedback, and

an external synchronizing circuit 15 for receiving an external reference signal As with the above, the PC 10 contains a CPU, ROM, RAM, and other interfaces, but these functional parts are omitted in the drawing Further, the PC 10 environment allows execution of video editing software for editing at least data in DV format, and output is performed via the DV data processing unit 11 and IEEE 1394 circuit 12.

[0053] The DV converter 20 comprises the IEEE1394 circuit 21 for receiving a video signal in DV format transferred via the IEEE1394 cable 30, the data conversion circuit 23 for converting the transferred video signal in DV format into an analog video signal or SDI video signal, and a clock source 26 constituted by a crystal oscillator or the like. This DV converter also comprises a CPU, ROM, RAM, and various interfaces, but these functional parts are omitted in the drawing

[0054] With the third embodiment thus configured, in accordance with a reference signal received by the external synchronizing circuit 15 of the PC 10, the VCXO 14 in the PC 10 is subject to feedback control so as to maintain a constant timing differential between the reference signal and cycle start packet. As a result, the output interval between cycle start packets created by frequency division at a set rate of the VCXO 14 clock changes, and the transfer rate from the 1394OHCI compliant IEEE1394 PC 10 determined by the cycle start packet interval is synchronized with the reference signal. In this case, the IEEE1394 node that is the PC 10 needs to serve as a cycle master.

[0055] Thus, with the third embodiment, a data-converted analog video signal or SDI video signal is fully synchronized with the reference signal and output in a state with no defects such as dropped frames or repeated frames.

[0056] With the third embodiment, standard hardware can serve as the DV converter 20 without modification).

[0057] Thus, with the present invention, the frame frequency of data output in synchronism with a reference signal for external synchronization, and of data output via the 1394OHCI compliant IEEE 1394 interface can be synchronized, preventing data defects caused by difference in frame frequencies such as dropped frames or repeated frames.

Industrial Applicability

[0058] With the present invention, when a video signal in DV format is output from a PC and converted into an analog video signal or SDI video signal, the IEEE 1394 transfer rate and output frame rate are synchronized, preventing the occurrence of image defects such as dropped frames or repeated frames. The data formats for conversion are not limited to those described in the embodiments, and application is possible to mutual conversion between video signals in such formats as analog video signal, SDI video signal, DV video signal, MPEG1, MPEG2, MPEG4, and others Further, application of the present invention is not limited to moving image data, and application to audio data is also possible.

Claims

1. A data conversion system wherein one of first and second nodes on an IEEE1394 bus serves as a cycle master, first data is transferred from the first node to the second node in synchronism with a cycle start packet output from the cycle master, and second data generated by conversion of the first data in the second node is synchronized with an external reference signal and output, comprising:

   an external synchronizing signal receiver for receiving an external reference signal provided on at least one of the first and second nodes; and

   a synchronization adjustment unit for synchronizing the frequency of the cycle start packet output from the cycle master with the frequency of the reference signal received by the external synchronizing signal receiver

2. The data conversion system according to claim 1, wherein the first node is hardware comprising a 1394OHCI compliant IEEE1394 interface for outputting a video signal in DV format as first data, and the second node is data conversion hardware for outputting an analog video signal or SDI video signal as second data.

3. The data conversion system according to either one of claim 1 or claim 2, wherein the second node comprises the external synchronizing signal receiver and synchronization adjustment unit, and serves as cycle master for data transfer.

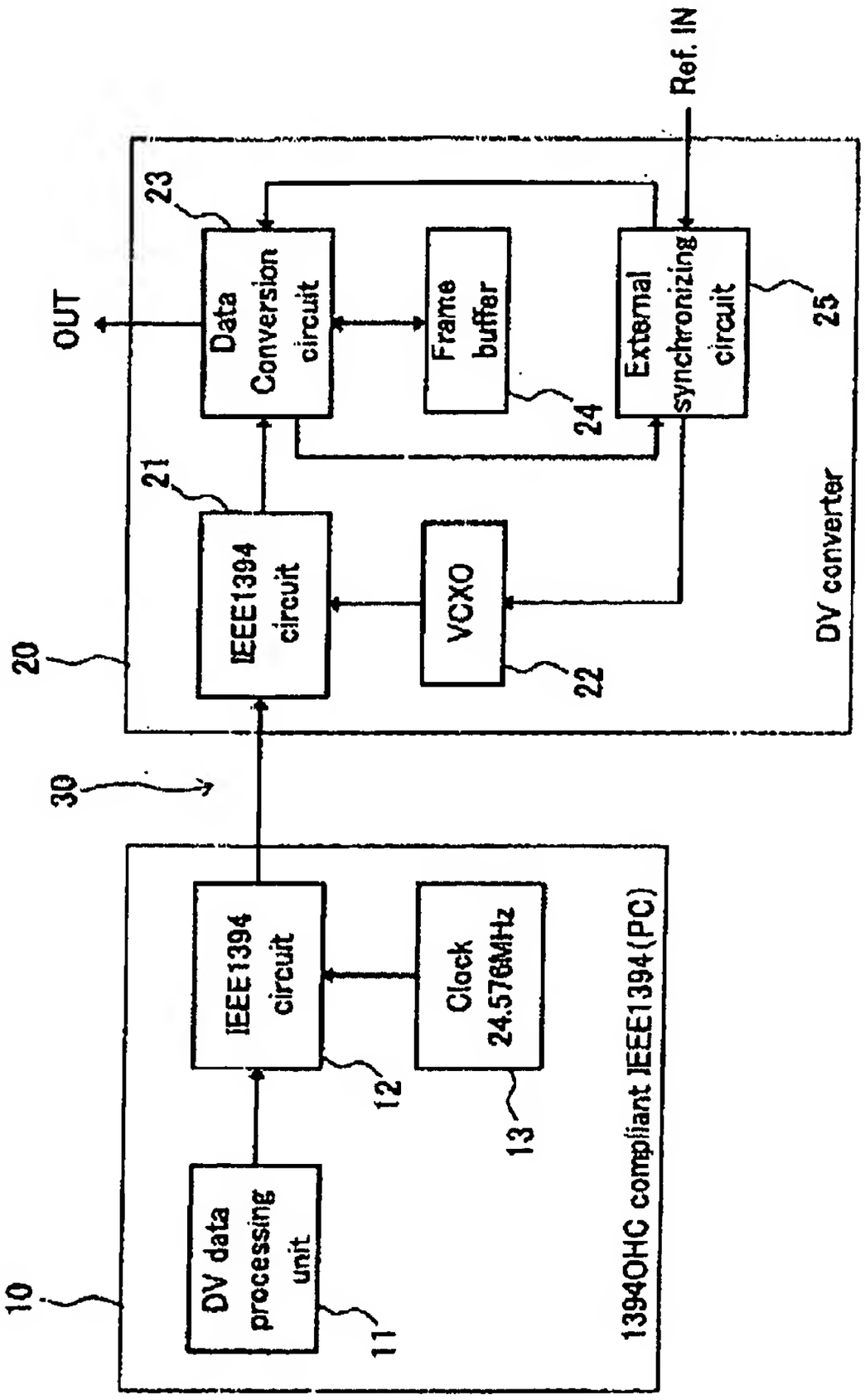
4. The data conversion system according to either one of claim 1 or claim 2, wherein the first node comprises the synchronization adjustment unit, the second node comprises the external synchronizing signal receiver and synchronization adjustment unit, and the cycle start packet frequency is synchronized with the frequency of the reference signal received by the external synchronizing signal receiver by means of the synchronization adjustment unit of the node that serves as cycle master.

5. The data conversion system according to claim 4, wherein when the first node serves as cycle master, the reference signal received by the external synchronizing signal receiver of the second node is transmitted from the second node to the first node by asynchronous transfer of the IEEE1394 interface

6. The data conversion system according to claim 4, comprising a dedicated synchronization signal line

for transmitting the reference signal received by the external synchronizing signal receiver of the second node from the second node to the first node when the first node serves as cycle master.

7. The data conversion system according to either one of claim 1 or claim 2, wherein the first node comprises the external synchronizing signal receiver and synchronization adjustment unit, and serves as cycle master for data transfer


Ref. IN
23
OUT
Data Conversion circuit
Frame buffer
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External synchronizing circuit
25
DV converter
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IEEE1394 circuit
VCXO
22
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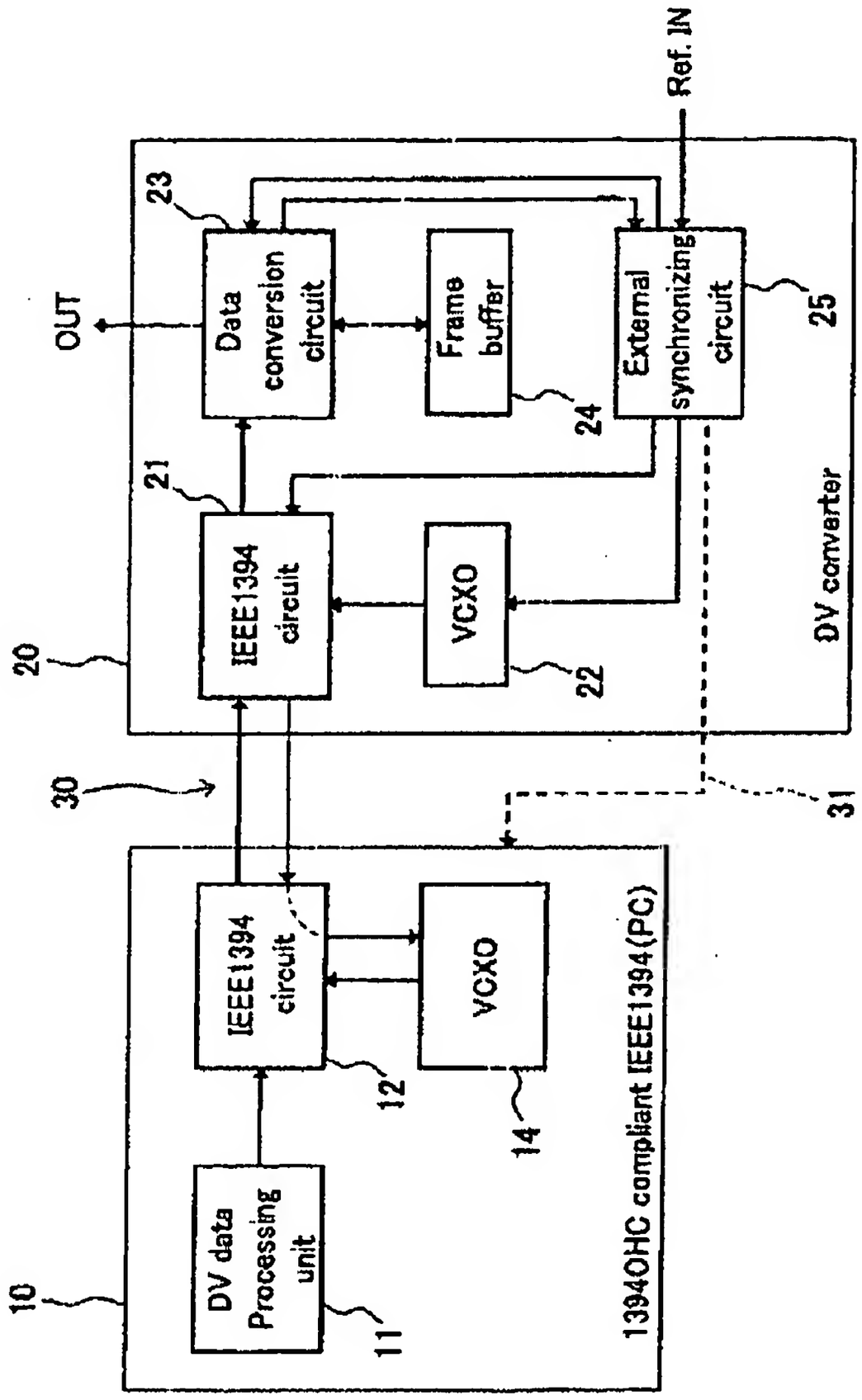
IEEE1394 circuit
12
Clock 24.576MHz
13
1394OHC compliant IEEE1394(PC)
10
DV data processing unit
11

Fig. 1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Data conversion circuit
Frame buffer
External synchronizing circuit
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24
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IEEE1394 circuit
VCXO
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VCXO
12
14
DV data Processing unit
11
10
1394OHC compliant IEEE1394(PC)

Fig. 2

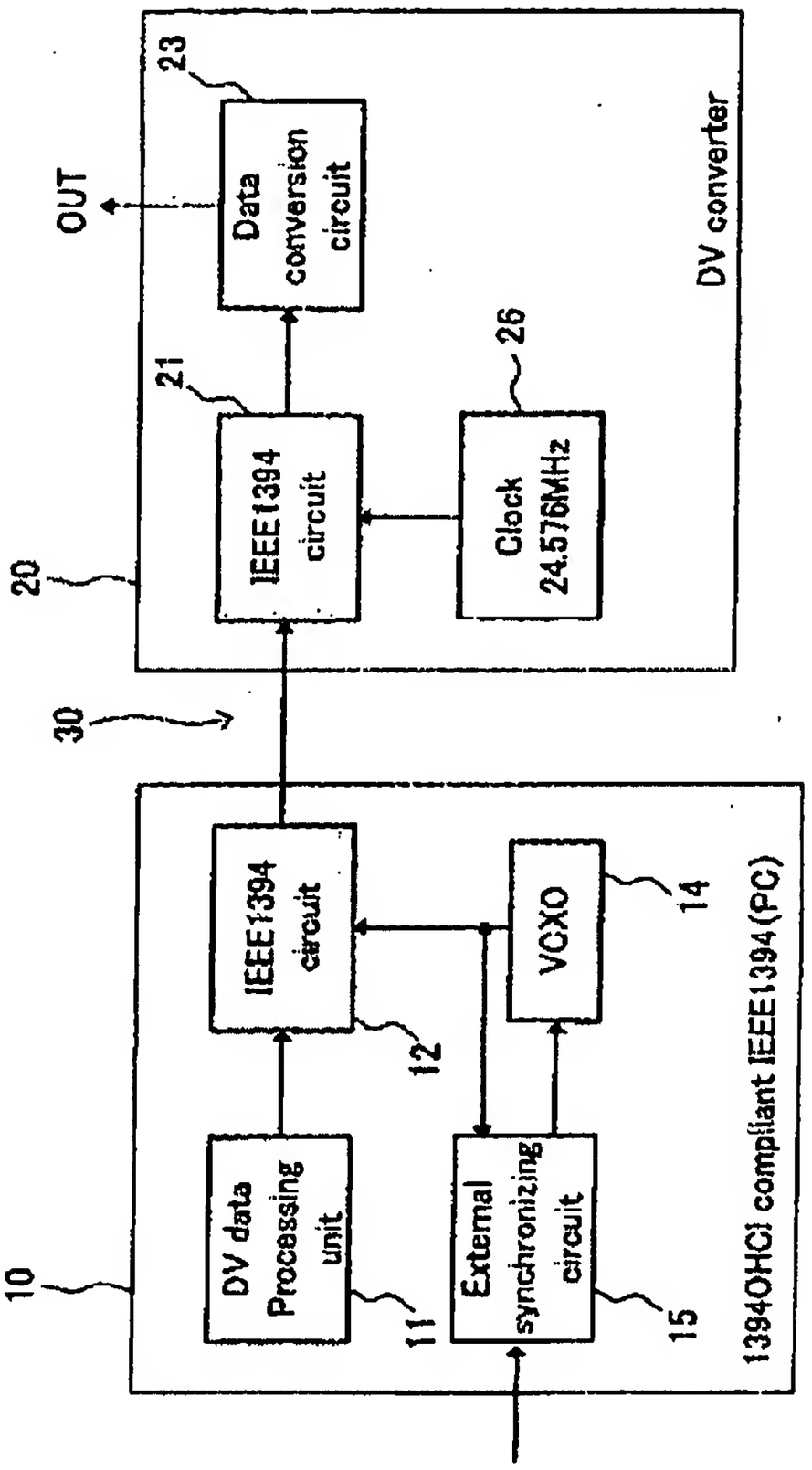
OUT
23
Data conversion circuit
DV converter
26
21
IEEE1394 circuit
Clock 24.576MHz
20
30
IEEE1394 circuit
VCXO
14
12
DV data Processing unit
External synchronizing circuit
11
15
10
1394OHCI compliant IEEE1394(PC)

Fig. 3

Ref. IN

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/11949

A CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H04N5/91

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H04N5/76-5/956

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-2003
Kokai Jitsuyo Shinan Koho 1971-2003 Jitsuyo Shinan Toroku Koho 1996-2003

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2002-271773 A (Matsushita Electric Industrial Co., Ltd.), 20 September, 2002 (20.09.02), Full text; Figs. 1 to 21 (Family: none)	1-7
A	JP 2000-32391 A (Canopus Co., Ltd.), 28 January, 2000 (28.01.00), Full text; Figs. 1 to 4 & EP 954174 A2	1-7
A	JP 2000-278644 A (Canopus Co., Ltd.), 06 October, 2000 (06.10.00), Full text; Figs. 1 to 10 (Family: none)	1-7

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 December, 2003 (10.12.03)	24 December, 2003 (24.12.03)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1998)